

U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	SNDK.006USQ	09/114,504
	Applicants	Conf. No.
	Harari et al.	9326
	Filing Date	Group
	July 13, 1998	2824

U.S. Patent Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

U.S. Published Patent Application Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents

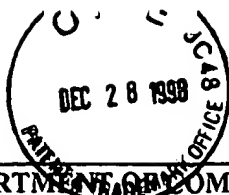
						Translation	
	Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

ju	1	European Search Report, corresponding European Application No. 95107965.6-2210, July 7, 2003, 2 pages.
ju	2	Wilson, Ron, "1-Mbit Flash Memories Seek Their Role in System Design", Computer Design, Vol. 28, No. 5, 1 March 1989, 2 pages.
ju	3	Kuo, Clinton, et al., "A SUB 100ns 32K EEPROM", Proceedings of the National Electronics Conference, Vol. 36, 1982, page 390.

Examiner	Vu Le	Date Considered	11/22/04
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

FORM PT01449
(REV. 8-83)U.S. DEPARTMENT OF COMMERCE
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ATTY. DOCKET NO.

HARI.006USQ

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ELIYAHOU HARARI et al.

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
84	A1	3 8 9 5 3 6 0	7/75	Cricchi et al.			
	A2	3 8 9 8 6 3 2	8/75	Spencer, Jr.			
	A3	3 9 0 6 4 5 5	9/75	Houston et al.			
	A4	3 9 1 4 7 5 0	10/75	Hadden, Jr.			
	A5	4 0 4 4 3 3 9	8/77	Berg			
	A6	4 0 5 8 7 9 9	11/77	George et al.			
	A7	4 0 6 4 4 0 5	12/77	Cricchi et al.			
	A8	4 1 1 5 8 5 0	9/78	Houston et al.			
	A9	4 1 3 0 8 9 0	12/78	Adam			
	A10	4 1 4 1 0 8 1	2/79	Horne et al.			
94	A11	4 1 9 3 1 2 8	3/80	Brewer			

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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
94	B1	JP 58 0 8 6 7 7 7	1983	Japan			Abstract
	B2	JP 58 2 1 5 7 9 4	1983	Japan			Abstract
	B3	JP 58 2 1 5 7 9 5	1983	Japan			Yes
	B4	JP 59 1 6 2 6 9 5	1984	Japan			Abstract
94	B5	JP 62 2 8 3 4 9 7	1987	Japan			Abstract

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94	C1	Flash Memory Cards, Oct. 1992, pp. 4-91, 4-95, and 4-96.
94	C2	Cricchi et al., "Nonvolatile Block-Oriented RAM", IEEE International Solid-State Circuits Conference, Feb, 13-15, 1974, Digest of Technical Papers.
94	C3	Brewer et al., "Block-Oriented Random Access MNOS Memory", National Computer Conference and Exposition, Chicago, May 6-10, 1974, AFIPS Conference Proceedings, vol 43. Pp. 837-840.

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ju	A12 4 2 4 1 4 2 4	12/80	Dickson et al.			
	A13 4 4 1 2 3 0 9	10/83	Kuo			
	A14 4 4 2 8 0 4 7	1/84	Hayn et al.			
	A15 4 4 3 3 3 8 7	2/84	Dyer et al.			
	A16 4 5 2 7 2 5 7	7/85	Cricchi			
	A17 4 8 6 0 2 6 2	8/89	Chiu			
	A18 4 8 8 2 6 4 2	11/89	Tayler et al.			
	A19 4 8 8 7 2 3 4	12/89	Iijima			
	A20 4 9 2 0 4 7 8	4/90	Furuya et al.			
	A21 4 9 3 1 9 9 7	6/90	Mitsuishi et al.			
ju	A22 4 9 3 3 9 0 6	6/90	Terada et al.			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
B6 JP 59 1 8 6 0 1 5	1984	Japan			Abstract
B7 JP 62 2 8 3 4 9 6	1987	Japan			Yes
B8 JP 63 1 8 3 7 0 0	1988	Japan			Abstract
B9 JP 58 0 8 6 7 7 7	1983	Japan			Abstract
B10 JP 52 0 0 8 7 3 8	1977	Japan			Abstract

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ju	C4	Brewer et al., Low Cost MNOS BORAM", Proceedings of IEEE National Aerospace Electronics Conference, NAECON '77, May 17-19, 1977.
ju	C5	Short, "Microprocessors and Programmed Logic", second edition. Ch 13.2.2 Electrically Erasable Programmable Read only Memory, EEPROM Prentice Hall International, 1987.
ju	C6	Fitzpatrick et al., "MNOS/SOS Memory Using High-Voltage Depletion-Mode CMOS Logic", Westinghouse Electric Corp., pp. 196-199.
	C7	SEEQ Technology Incorp., 48F512 512 Flash EEPROM, Preliminary Data Sheet, Oct 1988, pp. 2-1, 2-24.

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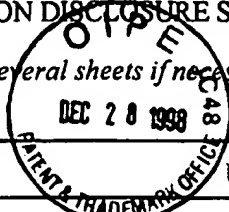
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ju	A23 4 9 4 9 3 0 9	8/90	Rao			
	A24 5 0 5 3 9 9 0	10/91	Kreifels et al.			
	A26 5 0 8 4 8 4 3	1/92	Mitsuishi et al.			
	A27 5 2 2 4 0 7 0	6/93	Fandrich et al.			
	A28 5 2 6 7 2 1 8	11/93	Elbert			
	A29 5 3 0 1 1 6 1	4/94	Landgraf et al.			
	A30 5 3 4 1 3 3 0	8/94	Wells et al.			
	A31 5 3 6 3 3 3 4	11/94	Alexander et al.			
	A32 5 4 1 8 7 5 2	5/95	Harari et al.			
	A33 5 6 4 8 9 2 9	7/97	Miyamoto			
ju	A34 5 7 1 9 8 0 8	2/98	Harari et al.			

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ju	B11 EP 0 2 8 3 2 3 8	1988	EPO			
ju	B12 JP 63 1 0 6 9 8 9	1988	Japan			Abstract
ju	B13 JP 63 2 2 5 9 9 9	1988	Japan			Abstract

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ju	C8	Intel Corporation, 27F256 256K (32K x 8) CMOS Flash Memory", Data Sheet, May 1988, pp. 1-21.
ju	C9	Cricchi et al., "The Drain-Source Protected MNOS Memory Device and Memory Endurance", IEDM Technical Digest, 1973, pp. 126-129.
ju	C10	Cormier, "Erasable/Programmable Solid-State Memories", EDN, pp. 145-154, November 14, 1985, pp. 145-154.

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ju	A35 4 5 2 1 8 5 3	6/85	Gutttag			
	A36 4 4 6 8 7 2 9	8/84	Schwartz			
	A37 4 9 3 9 6 9 0	7/90	Momodomi et al.			
	A38 4 9 5 3 1 2 9	8/90	Kobayashi et al.			
	A39 5 0 3 3 0 2 3	7/91	Hsia et al.			
	A40 4 8 6 0 2 2 8	8/89	Carroll			
	A41 4 8 1 1 2 9 3	3/89	Knothe et al.			
	A42 4 7 9 6 2 3 5	1/89	Sparks et al.			
	A43 4 7 5 8 9 8 8	7/88	Kuo			
	A44 4 7 5 8 9 8 6	7/88	Kuo			
ju	A45 4 6 8 5 0 8 4	8/87	Canepa			

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ju	C11	Cernea et al., "A 1Mb Flash EEPROM", 1989 IEEE International Solid-State Circuits Conference.
ju	C12	Wilson, "1-Mbit Flash Memories seek their role in System Design", Computer Design, March 1, 1989, pp. 30 and 32.
ju	C13	Kynett et al., "An In-System Reprogrammable 32KX8 CMOS Flash Memory", IEEE J. Solid-State Circuits, vol. 23, No. 5, October 1988, pp. 1157-1163.

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ge	A46 4 8 3 9 7 0 5	6/89	Tigelaar et al.			
	A47 4 7 8 0 8 5 5	10/88	Iida et al.			
	A48 5 2 6 8 8 7 0	12/93	Harari			
	A49 5 1 6 8 4 6 5	12/92	Harari			
	A50 4 8 6 0 2 6 1	8/89	Kreifels et al.			
	A51 4 8 1 1 2 9 4	3/89	Kobayashi et al.			
	A52 4 7 6 3 3 0 5	8/88	Kuo			
	A53 5 0 4 3 9 4 0	8/91	Harari			
	A54 4 4 6 0 9 8 2	7/84	Gee et al.			
	A55 4 8 0 5 1 5 1	2/89	Terada et al.			
ge	A56 4 0 9 0 2 5 8	5/78	Cricchi			

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Vu	A57	4	8	4	1	4	8	2		6/89	Kreifels et al.	—	—	

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